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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,715	03/15/2004	Toyokazu Fujii	60188-756	8984

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,715	FUJII ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/07/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34,36,37 and 40-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34,36,37 and 40-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Amendment dated 12/07/2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 34, 36-37 and 42-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato et al. [US 5,605,867].

► With respect to claims 34, 36-37 and 43, Sato et al. (fig. 13, col. 24) discloses the claimed semiconductor device comprising:

a substrate (81) having a semiconductor region ***[claims 34 and 43]***;

an insulating film (82, BPSG, col. 24 line 2) formed over said semiconductor region, said insulating film including impurities comprising boron and phosphorous and inherently having a property of reflowing due to a heat treatment under predetermined conditions ***[claims 34, 36-37 and 43];***

an interconnection (83, col. 24 lines 2-3) disposed on and in contact with a first region of an upper surface of said insulating film (82) ***[claims 34 and 43];***

a silicon oxide film (84, plasma TEOS CVD NSG, col. 24 lines 2-3) in contact with a second region of said upper surface of said insulating film, said silicon oxide film inherently having a property of not reflowing due to said heat treatment under predetermined conditions (*BPSG is reflowed at a temperature lower than that of the plasma TEOS CVD NSG; the plasma TEOS CVD NSG has a property of not reflowing due to a heat treatment of the temperature at which the BPSG is reflowed)* ***[claims 34 and 43];*** and

a silicon nitride film (88, col. 24 lines 45) formed on said insulating film (82) and said interconnection (83) ***[claims 34 and 43];***.

► With respect to claim 42, Sato et al. (fig. 13, col. 24) discloses that a part of the silicon oxide film (84) formed over the interconnection (83); and a part of silicon nitride film (88) formed on said silicon oxide film (84).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 34, 36-37, 40-46 and 48, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (fig. 16 and page 2) in view of Fazan et al. [US 5,597,756] previously applied.

► With respect to claims 34, 36-37 and 43, Applicant Admitted Prior Art (fig. 16 and page 2) discloses the claimed semiconductor device comprising:

a substrate (1, silicon substrate) having a semiconductor region ***[claims 34 and 43]***;

an insulating film (48, BPSG, page 2 lines 7-9) formed over said semiconductor region, said insulating film including impurities comprising boron and phosphorous and inherently having a property of reflowing due to a heat treatment under predetermined conditions ***[claims 34, 36-37 and 43];***

an interconnection (49, page 2 lines 10-12) disposed on and in contact with a first region of an upper surface of said insulating film (48) ***[claims 34 and 43];***

a silicon nitride film (50) ***[claims 34 and 43]*** formed on said insulating film (48) and said interconnection (49).

Applicant Admitted Prior Art fails to disclose a silicon oxide film in contact with a second region of said upper surface of said insulating film, said silicon oxide film having a property of not reflowing due to said heat treatment under said predetermined conditions (*said silicon oxide film is not reflowed at the predetermined condition at which said insulating film BPSG is reflowed*) wherein the silicon nitride film formed on said silicon oxide film ***[claims 34 and 43]***. Saying another way, APA fails to discloses the silicon oxide film between and in contact with the upper surface of said insulating film (BPSG) and the lower surface of the silicon nitride wherein said silicon oxide film is not reflowed at the predetermined condition at which said insulating film (BPSG) is reflowed.

However, Fazan et al (fig 8, col. 3 lines 60-64 and col 4 lines 6-11) discloses the silicon oxide film (21, TEOS silicon dioxide) in contact with the upper surface of the insulating film (16, BPSG), said silicon oxide film (TEOS silicon dioxide) inherently having a property of not reflowing due to said heat treatment under said predetermined

conditions for reflowing the insulating film (16, BPSG) (*BPSG is reflowed at a temperature lower than that of the TEOS silicon dioxide; the TEOS silicon dioxide is not reflowed at a temperature at which said insulating film BPSG is reflowed*) wherein the silicon nitride film (22) formed on said silicon oxide film (21). Saying another way, Fazan et al discloses the silicon dioxide film (21, TEOS silicon dioxide) formed between and in contact with the upper surface of said insulating film (16, BPSG) and the lower surface of said silicon nitride film (22) wherein said silicon oxide film (21, TEOS silicon oxide) is not reflowed at the predetermined condition at which said insulating film (BPSG) is reflowed.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify the device of Applicant Admitted Prior Art by using the silicon oxide film as being claimed, per taught by Fazan et al, to provide a better semiconductor device with reduced stress between the insulating film (borophosphosificate glass) and the silicon nitride film (see Fazan et al , col. 4 lines 6-9). By doing so, problem of crack to the device will be reduced.

► With respect to claims 40-41, as reason given above, Fazan et al. (fig. 8) further discloses wherein substantially the entire lower surface of said silicon nitride film (22) is in contact with an upper surface of said silicon oxide film (21). It would have been obvious for those skilled in the art to have the semiconductor device of APA in view of Fazan et al with the silicon nitride film and the silicon oxide film as being claimed -- wherein substantially the entire lower surface of said silicon nitride film is in contact with an upper surface of said silicon oxide film – to reduce stress between the insulating film and the silicon nitride film for preventing problem of crack in the semiconductor device.

► With respect to claim 42, as reason given above, Fazan et al. (fig. 8) further discloses that a part of the silicon oxide film (21) formed over the interconnection (18B); and a part of silicon nitride film (22) formed on said silicon oxide film (21). It would have been obvious for those skilled in the art to have the semiconductor device of APA in view of Fazan et al with a part of said silicon oxide film formed over said interconnect and a part of said silicon nitride formed on said silicon oxide film, as being claimed, to reduce problem of stress in semiconductor device.

► With respect to claim 44, Applicant Admitted Prior Art (fig. 16, page 2 lines 15-17) discloses that an upper insulating film (51) including impurities is formed on the silicon nitride film (50).

► With respect to claim 45, Applicant Admitted Prior Art (fig. 16) discloses a surface of the upper insulating film (51) is planarized.

► With respect to claim 46, in the combination of the semiconductor device of APA in view of Fazan et al, it would have been obvious for those skilled in the art to have the silicon oxide film (21) providing tensile stress for said silicon nitride.

► With respect to claim 48, Applicant Admitted Prior Art (fig. 16) discloses a gate electrode (47) is formed over said semiconductor region (1) and said insulating film (48) is formed over said gate electrode (47).

3. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (fig. 16 and page 2) in view of Fazan et al. [US 5,597,756] as applied to claim 43 above, further in view of Douglas [US 4,807,016] previously applied.

Applicant Admitted Prior Art in view of Fazan et al. substantially discloses all the limitations as claimed above except teaching that the insulating film includes phosphorus which concentration is 3.0 wt% or more. However, Douglas discloses that the insulating film (BPSG) typically includes approximately 1 to 10 by weight of phosphorus in their chemical formula (see col. 1, lines 39-43). The concentration range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Therefore, at the time of invention, it would have been obvious to the skilled in the art, in view of Douglas, to use the insulating film including concentration of 3.0% or more in the semiconductor device of Ueda et al. to provide isolation function as desired in the semiconductor device.

Response to Arguments

4. Applicant's arguments with respect to claims 34, 36-37 and 40-48 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanhha Pham